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PPLICATION NO. FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/082,144	02/25/2002	Victor Roberts Augsburg	RPS920010176US1	2686	
45211 7.	590 09/01/2004		EXAMINER		
KELLY K. K	LLY K. KORDZIK		COLEMAN, ERIC		
WINSTEAD S PO BOX 50784	ECHREST & MINICK PC		ART UNIT	PAPER NUMBER	
DALLAS, TX 75201			2183	·	
			DATE MAILED: 09/01/2004		

Please find below and/or attached an Office communication concerning this application or proceeding.



		Application	on No.	Applicant(s)				
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Office Action Summary		10/082,14		Augsburg et al.	•			
	Jinoo Aodon Odiniidi y	Examine:		2183				
	The MAILING DATE of this commun	Eric Cole			ress			
Period fo		on an		<u> </u>				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).								
Status								
1)	Responsive to communication(s) file	ed on						
2a)☐	This action is FINAL .	2b)⊠ This action is r						
3)□								
Dispositi	ion of Claims							
5)□ 6)⊠ 7)□ 8)□ Applicat 9)□	Claim(s) 1-51 is/are pending in the a 4a) Of the above claim(s) is/a Claim(s) is/are allowed. Claim(s) 1-51 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction Papers The specification is objected to by the drawing(s) filed on is/are	re withdrawn from co	requirement.	e Examiner				
10)[
11)	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority :	under 35 U.S.C. § 119							
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 								
2) Notice 3) Information Paper	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (mation Disclosure Statement(s) (PTO-1449 of the Process of the	РТО-948) г РТО/SB/08)	4) Interview Summ Paper No(s)/Mai 5) Notice of Inform 6) Other:		-152)			

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35
 U.S.C. 102 that form the basis for the rejections under this section made in this
 Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1,5,8,16,19,27,30,38,41,49 are rejected under 35 U.S.C. 102(b) as being anticipated by Witt (patent No. 6,167,506).
- 3. Witt taught (claims 1,8,19,30,41) the invention as claimed including a data processing ("DP") system comprising: fetching a branch instruction from memory, wherein the branch instruction stores an offset of a target address comprising n bits; calculating n-1 least significant bits of the target address of the branch instruction; and replacing n-1 least significant bits of the target address of the branch instruction (e.g., see figs. 2,4,4a; col. 3, line 64-col. 4, line 37; col. 21, lines 13-40; and col. 23, lines 3-63).
- 4. As to further limitations of claims 8,19,30 (the instruction memory and cache) Witt taught instruction queue (20) and instruction memory (80) caches (14,16,38) and main memory 204) (e.g., see figs. 1,15) and encoder (106) (e.g., see fig.4a) and col. 21, lines 13-48).
- 5. As per claims (5,16,27,38,49) Witt taught the calculating comprising adding a value stored the value in the least significant bits of the offset of the target address stored in the branch instruction with a value stored in the n-1 least

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significant bits of the address of the branch instruction (e.g., see col. 22, lines 4-30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 2-4,6-7,9-15,17,18,20-26,28,29,31-37,39,40,42-48,50,51 rejected under 35 U.S.C. 103(a) as being unpatentable over Witt as applied to claims 1,8,19,30,41 above, and further in view of Boutaud (patent No. 5,907,714).
- 7. Boutaud taught (claims 2,9,20,31,42) inserting status bits (1021) including a carry bit into the branch instruction (e.g., see figs. 31,32,35 and col. 46, lines 5-46).
- 8. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Witt and Boutaud. One of ordinary skill would have been motivated to incorporate the Boutaud teachings of including status bits into the branch instructions to provide for a more efficient way to test for branch status condition since the condition bit would have been readily available.
- 9. As per claims 3, Witt taught storing a branch instruction storing the n-1 least significant bits of the target instruction, retrieving the branch instruction storing the n-1 least significant bits of the target and selecting the one of a set of

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upper order bit value combinations of the address of the branch instruction (e.g., see col. 22, lines 40-65).

- 10. As per claims 3,10-14,21-25,32-36,43-47, the limitations of calculating a set of upper order bit value combinations one the branch instructions, Witt taught the received address was calculated by and adder (e.g., see col. 23, lines15-41).
- 11. As per the appending of the least significant bit with the upper order bits (claims 4,15,26,37,48) Witt taught the concatenating of the least significant bits and upper order bits (e.g., see col. 22, lines 49-65).
- 12. As per claims 6,7,17,18,28,29,39,40,50,51, One of ordinary skill would have been motivated to increment or decrement the upper bit value at least to address a separate block or segment of instructions that would have been used to separate the instructions from different processes (e.g., see col. 3, line 28-col. 4, line 36). Also one of ordinary skill would have motivated to use the status bits Boutaud in determining which upper address combination to selectively and efficiently allow for separation between processes and data integrity (e.g., see figs.34, 35 and col. 46, lines 5-46 of Boutaud).

Conclusion

Doing (patent No. 6,438,671) disclosed system generating partition corresponding read address in partitioned mode (e.g., see abstract).

Arora (patent No. 5,832,260) disclosed a processor for processing of instructions in a program including a conditional program flow control instruction (e.g., see abstract).

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Roberts (patent No. 6,279,106) disclosed a system for reducing branch target storage by calculating direct branch targets on the fly (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN PRIMARY EXAMINER